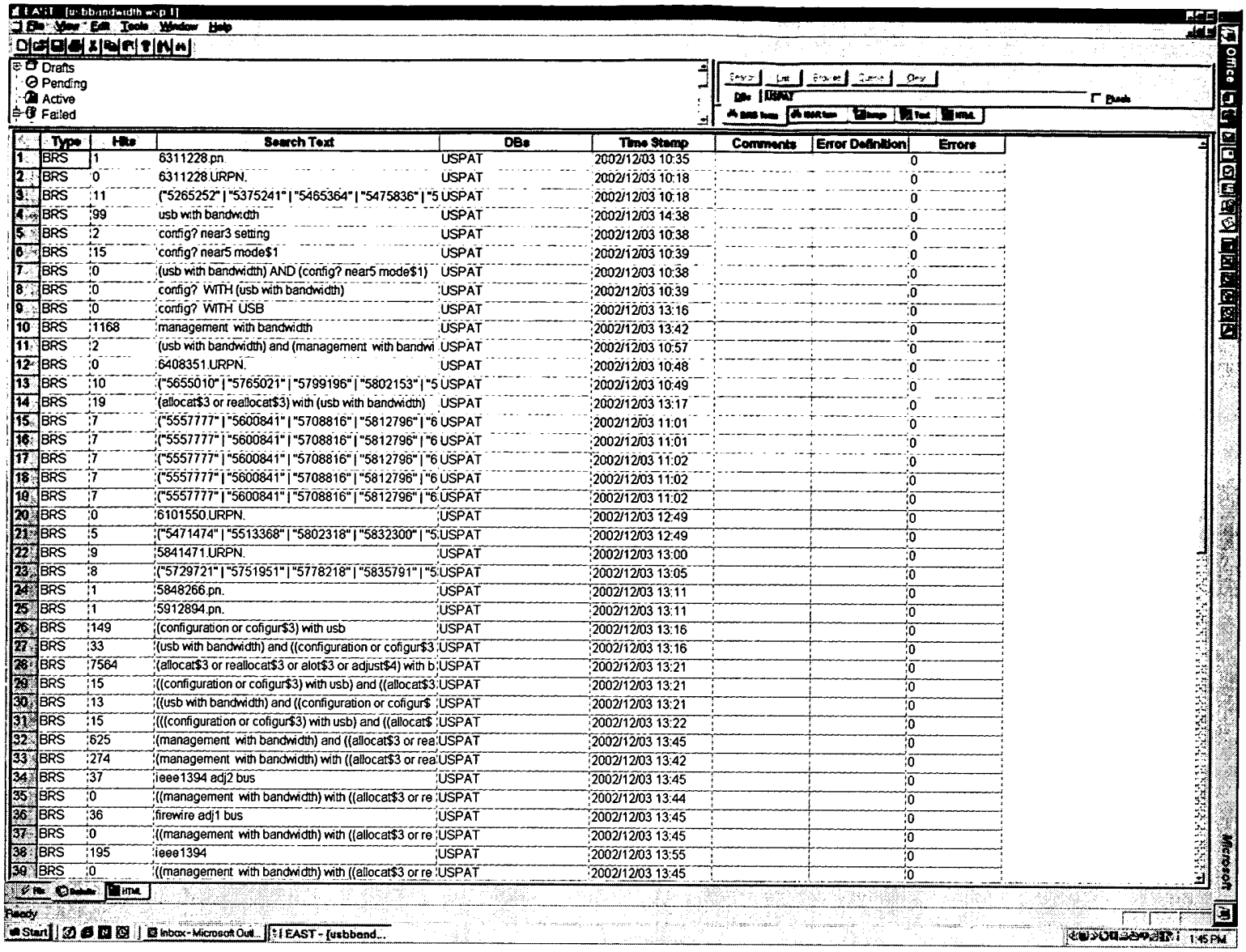

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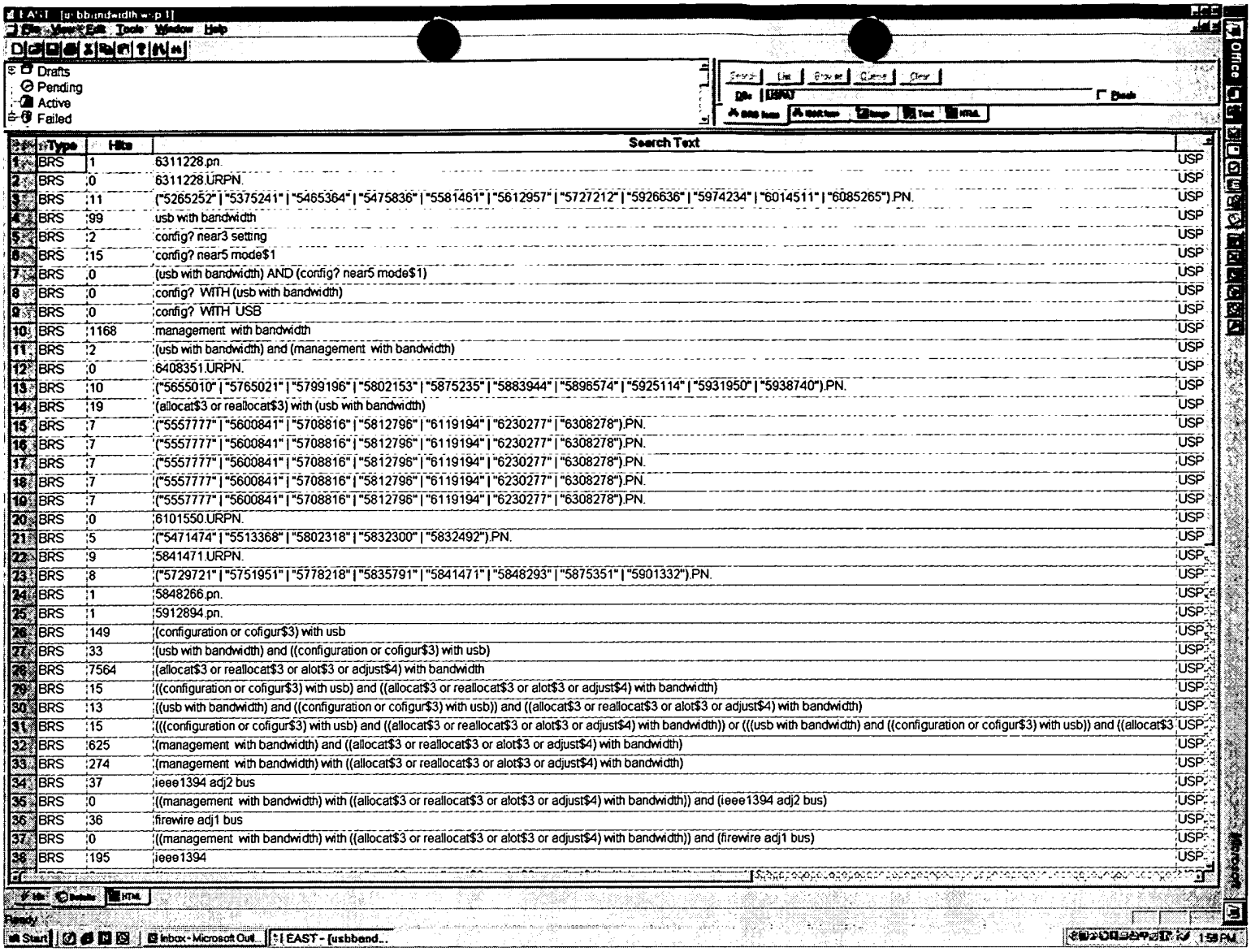
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5 BRS 2 config? near3 setting USP
6 BRS 15 config? near5 mode$1 USP
7 BRS 0 (usb with bandwidth) AND (config? near5 mode$1) USP
8 BRS 0 config? WITH (usb with bandwidth) USP
9 BRS 0 config? WITH USB USP
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36 BRS 36 firewire adj1 bus USP
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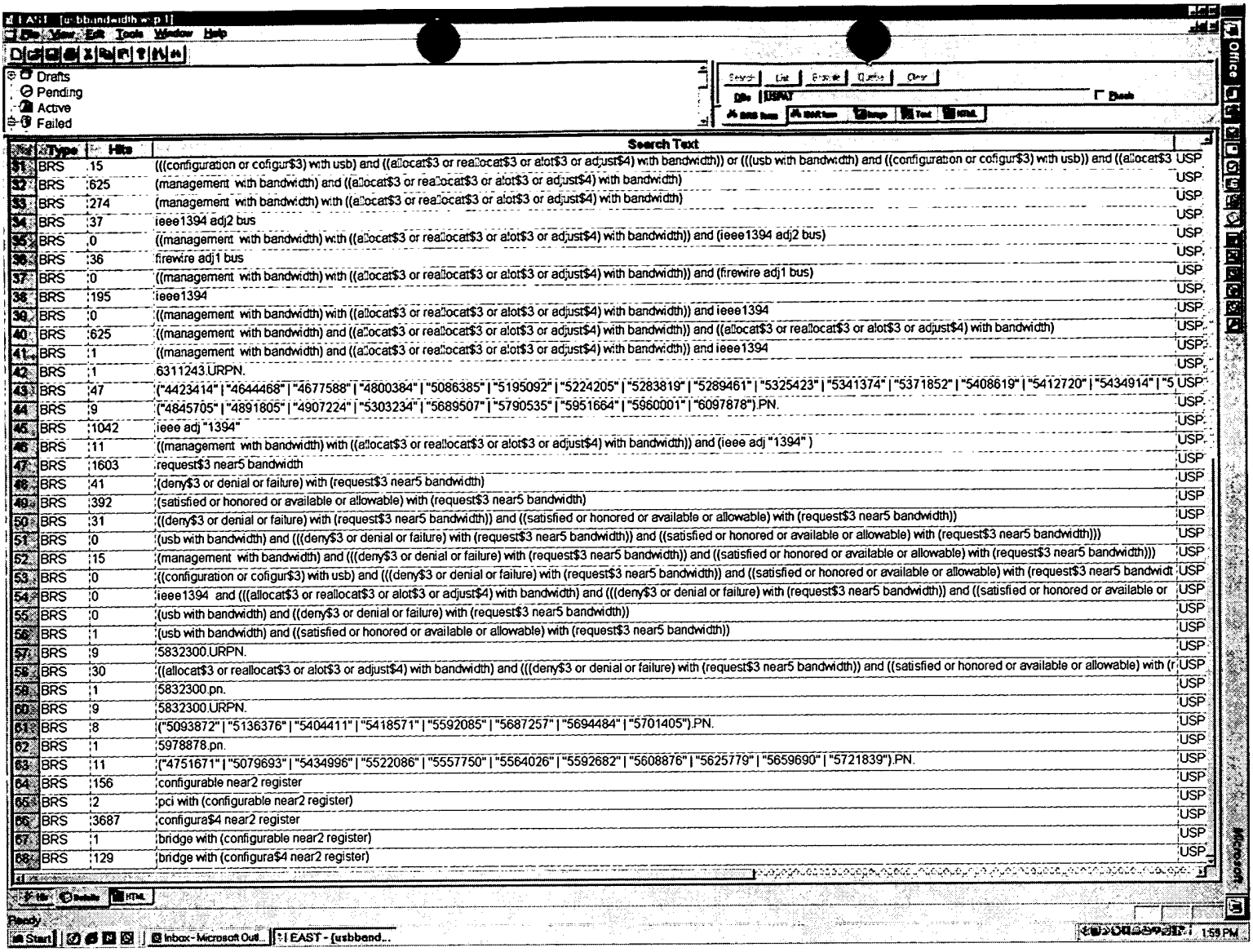

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68	BRS	41	(deny$3 or denial or failure) with (request$3 near5 bandwidth)	USP
69	BRS	392	(satisfied or honored or available or allowable) with (request$3 near5 bandwidth)	USP
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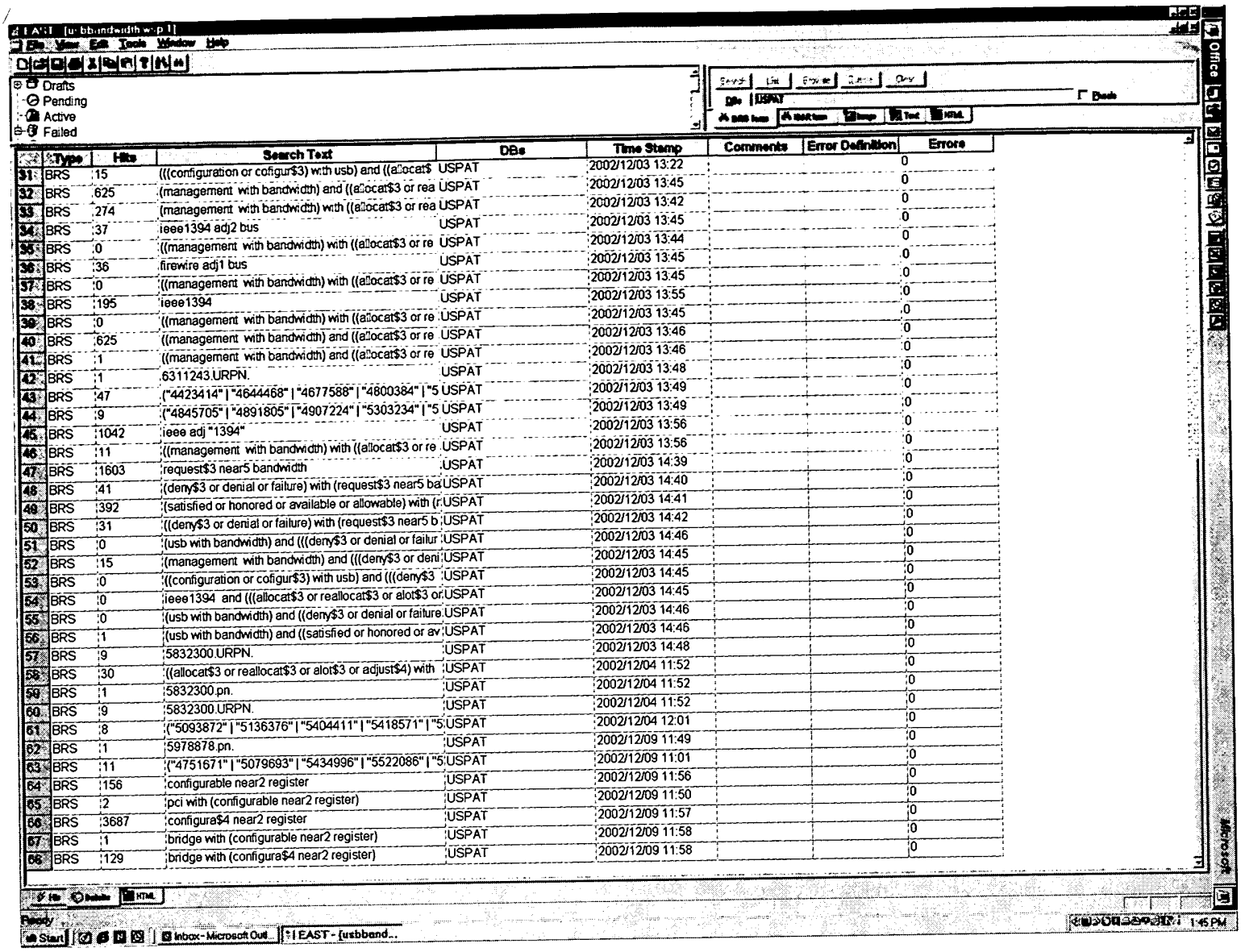
88	BRS	129	bridge with (configura$4 near2 register)	USP



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49	BRS	392	(satisfied or honored or available or allowable) with (r	USPAT	2002/12/03 14:41			0
50	BRS	31	((deny$3 or denial or failure) with (request$3 near5 b	USPAT	2002/12/03 14:42			0
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67	BRS	1	bridge with (configurable near2 register)	USPAT	2002/12/09 11:58			0
68	BRS	129	bridge with (configura$4 near2 register)	USPAT	2002/12/09 11:58			0

US-PAT-NO: 6212582

DOCUMENT-IDENTIFIER: US 6212582 B1

TITLE: Method for multi-priority, multicast flow control in a packet switch

---------- KWIC ---------

Detailed Description Text - DETX (5):

This hybrid flow control scheme provides various features including preventing
cell loss on the receive BIC buffers; maintaining a high throughput; achieving
MAX-MIN fairness in bandwidth allocation among streams if enough access
bandwidth is available to the streams; prohibiting high-rate streams from
unfairly starving low-rate streams which are subject to an access bandwidth
constraint; maintaining a low switching delay; requiring minimum utilization of
bus bandwidth, BIC buffer space and BIC processor for control purposes; and,
being simple to implement at the BIC and operate at high data rates up to the
bus speed.

FIG. 1

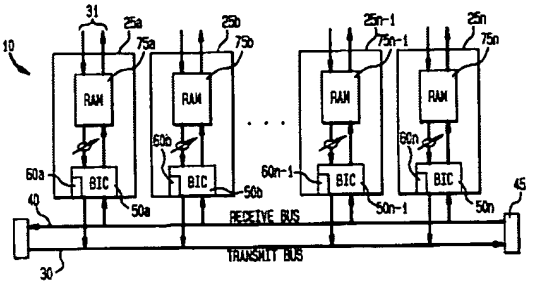
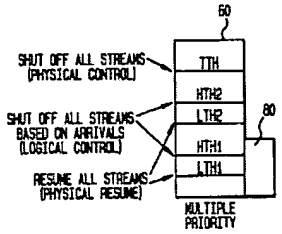


FIG. 2



US-PAT-NO: 5640519

DOCUMENT-IDENTIFIER: US 5640519 A

TITLE: Method and apparatus to improve latency experienced by an agent under a round robin arbitration scheme

---------- KWIC ---------

US PATENT NO. - PN (1):

5640519

US005640519A

United States Patent [19]
Langendorf et al.

[11] Patent Number: 5,640,519
[45] Date of Patent: Jun. 17, 1997

[54] METHOD AND APPARATUS TO IMPROVE LATENCY EXPERIENCED BY AN AGENT UNDER A ROUND ROBIN ARBITRATION SCHEME

[75] Inventors: Brian K. Langendorf, El Dorado Hills; James M. Dodd, Citrus Heights; George B. Hayek, Cameron Park, all of Calif.

[73] Assignee: Intel Corporation, Santa Clara, Calif.

[21] Appl. No.: 528,914

[22] Filed: Sep. 15, 1995

[51] Int. Cl.[6] G06F 13/364; G05F 13/362; G05F 13/36

[52] U.S. Cl. 395/291; 395/293; 395/729

[58] Field of Search 395/287, 288, 395/289, 290, 291, 293, 294, 296, 728, 729

[56] References Cited

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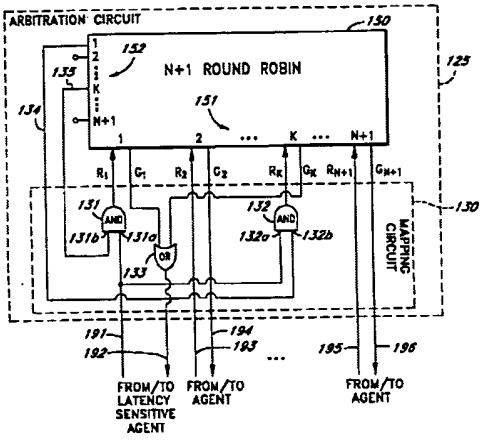
5,119,292	6/1992	Baker et al.	395/725
5,503,320	4/1994	Bach et al.	395/725
5,519,837	5/1996	Tran	395/291

Primary Examiner—Jack B. Harvey
Assistant Examiner—Ilgar Pauchidi
Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman

[57] ABSTRACT

An arbitration circuit which controls arbitration for a resource by a first plurality of agents including a latency sensitive agent. The arbitration circuit comprises a mapping circuit and an arbiter. The mapping circuit is coupled to the first plurality of agents in order to receive a resource request signal from the latency sensitive agent and thereafter produce a plurality of request signals identical to the resource request signal. These request signals are input into at least a first and second I/O ports of the arbiter. The arbiter, which is coupled to the mapping circuit, including a second plurality of I/O ports and a second plurality of control ports each corresponding to one of the I/O ports. The arbiter is configured to arbitrate request signals input into the second plurality of I/O ports including the plurality of request signals, to monitor which I/O port was last activated, and to deactivate a control port associated with the I/O port thereby producing a control signal. This control signal signals the mapping circuit to disable at least one of the plurality of request signals upon detecting that the control signal is associated with the first I/O port or the second I/O port.

24 Claims, 6 Drawing Sheets



Brief Summary Text - BSTX (18):

In more particular terms, the peripheral controller subsystem includes a microprogrammed processor which sets an indicator within the bus saturation detection apparatus to a predetermined state under microprogram control at the beginning of a transfer operation interval. The detector monitors the state of at least one predetermined signal utilized by the bus priority network for determining the extent of bus utilization. The detector apparatus switches the state of its indicator upon detecting the occurrence of an unused or available cycle. The output of the detector indicator is provided to branch test circuits included within the processor. At the end of the transfer interval, the subsystem tests the state of the saturation detector indicator. If the detector indicator specifies that the bus is not saturated, it resets the state of the indicator and begins another interval.

nt [19] [11] Patent Number: 5,099,420
[45] Date of Patent: Mar. 24, 1992

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d F. Getson, Jr.,
ll of Mass.
on Systems Inc.,

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5/325; 364/240.5;
364/DIG. 1
64/240.5; 370/85;
340/825.5

ENTS
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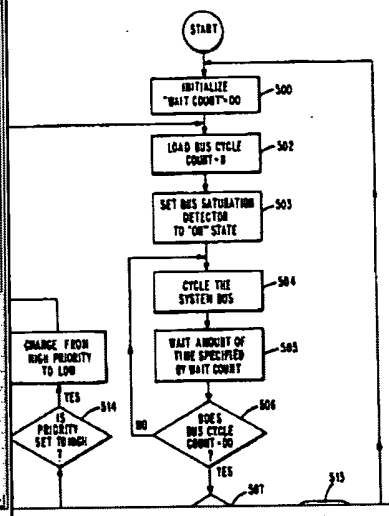
364/900
364/200

Primary Examiner—Salvatore Cangialosi
Attorney, Agent, or Firm—Faith F. Driscoll; John S. Solakian

[57] ABSTRACT

A plurality of units which are coupled to transfer requests, transfer data over an asynchronous bus network during allocated bus transfer cycles. The network has a tie-breaking bus priority network which is distributed to a common interface portion of each of the plurality of units and grants bus cycles and resolves simultaneous requests on a priority basis. At least one unit includes bus saturation detection apparatus included within its common interface portion for monitoring bus activity over established intervals of time. The detection of the occurrence of at least one available cycle over the given interval of time signals that the bus network is not in a saturated state. When the indicator specifies that the bus network is saturated, the unit throttles down its operation by increasing the amount of time between issuing data requests. Throttling continues until the bus is no longer being saturated.

24 Claims, 6 Drawing Sheets



Detailed Description Text - DETX (6):

The computer system architecture 10 also includes a bus monitoring apparatus
40. As described in detail below, the bus monitor 40 monitors a particular
peripheral device for a predetermined amount of time to determine the
effectiveness of bus transactions across the I/O bus 20 relative to the
particular peripheral device. The effectiveness of I/O bus transactions may be
measured in performance terms such as bus utilization, or bus efficiency. In
particular, the bus monitor 40 facilitates quantifying the utilization or
efficiency of the I/O bus 20 with regard to a particular peripheral device. As
described hereinafter, bus utilization is defined as a ratio of the total
number of clock cycles used for bus transactions across the I/O bus during a
predetermined time period or interval, to the total number of clock cycles
available for bus transactions across the I/O bus during the predetermined time
interval.

Detailed Description Text - DETX (7):

Likewise, bus efficiency is defined as a ratio of the total number of clock

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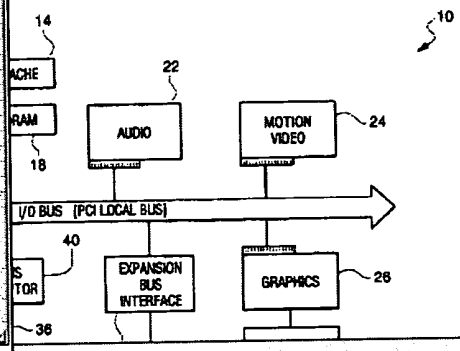
Primary Examiner—Ayaz R. Sheikh
Assistant Examiner—Eric Thlang
Attorney, Agent, or Firm—Paul J. Maginot; Wayne P. Bailey

[57] ABSTRACT

A method and apparatus for a method for measuring performance of an I/O bus. The method includes the steps of (a) determining a number of I/O bus clock cycles that occur during I/O bus transactions involving a peripheral device during a time period, and (b) determining a bus performance value for the I/O bus based on the number of I/O bus clock cycles determined in step (a). One embodiment of the apparatus includes a mechanism for determining a bus utilization value for the I/O bus based on the number of I/O bus clock cycles counted by the counter. Another embodiment of the apparatus includes a mechanism for determining a bus efficiency value for the I/O bus based on the number of I/O bus clock cycles counted by the counter.

17 Claims, 7 Drawing Sheets



US-PAT-NO: 6421348

DOCUMENT-IDENTIFIER: US 6421348 B1

TITLE: High-speed network switch bus

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Abstract Text - ABTX (1):

A network switch divides incoming frame data into cells. Each of the cells include a source identification field. Depending upon bandwidth availability and upon cell priority, the cells are transmitted over a switch bus. The cells are then routed based upon the source identification field. The network switch determines bandwidth usage by monitoring the switch bus. Upon detection of a start-of-frame cell, the network switch increments a bandwidth counter. Upon detection of an end-of-frame cell, the network switch adds an entry to a decrement FIFO. After a switch bus latency period, the network switch removes the entry from the decrement FIFO and decrements the bandwidth counter.

US006421348B1

(12) **United States Patent**
Gaudet et al.

(10) **Patent No.: US 6,421,348 B1**
(45) **Date of Patent: Jul. 16, 2002**

(54) **HIGH-SPEED NETWORK SWITCH BUS**

(75) Inventors: **Brian Gaudet**, Bethlehem, PA (US); **Vickie Pagano**, Sunnyvale; **Naveen Gopalakrishna**, Santa Clara, both of CA (US)

(73) Assignee: National Semiconductor Corporation, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/108,846

(22) Filed: Jul. 1, 1998

(51) Int. Cl.[7] H04L 12/28; H04L 12/56

(52) U.S. Cl. 370/401; 370/395.1; 370/235

(58) Field of Search 370/401, 402, 370/369, 395.1, 405, 412, 413, 419, 428, 229, 230, 395.42, 304, 360, 455

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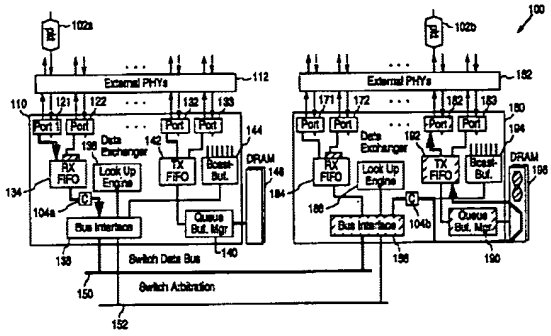
Primary Examiner—Doug Ton
Assistant Examiner—Brian Nguyen
(74) *Attorney, Agent, or Firm*—Stallman & Pollock LLP

(57) **ABSTRACT**

A network switch divides incoming frame data into cells. Each of the cells includes a source identification field. Depending upon bandwidth availability and upon cell priority, the cells are transmitted over a switch bus. The cells are then routed based upon the source identification field. The network switch determines bandwidth usage by monitoring the switch bus. Upon detection of a start-of-frame cell, the network switch increments a bandwidth counter. Upon detection of an end-of-frame cell, the network switch adds an entry to a decrement FIFO. After a switch bus latency period, the network switch removes the entry from the decrement FIFO and decrements the bandwidth counter.

17 Claims, 7 Drawing Sheets



PROGRAMMABLE TIMESLOT AND BANDWIDTH ALLOCATION CIRCUIT

[75] Inventor: **Harry J. Dyke, Oak Forest, Ill.**

[73] Assignee: **Rockwell International Corporation, El Segundo, Calif.**

[21] Appl. No.: **234,972**

[22] Filed: **Aug. 22, 1988**

[51] Int. Cl.[4] **H04J 3/16**

[52] U.S. Cl. **370/95.1**; 370/85.1; 340/825.51

[58] Field of Search 370/95, 96, 89, 90; 340/825.5, 825.51

[56] **References Cited**

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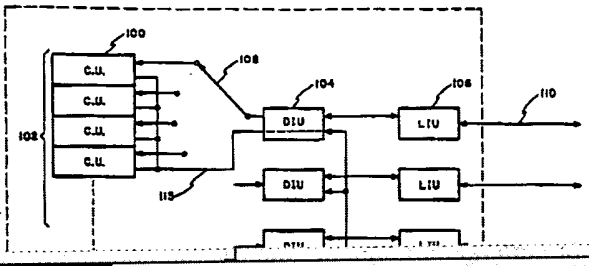
Primary Examiner—Douglas W. Olms
Assistant Examiner—Min Jung
F. Hamann

[57] **ABSTRACT**

A system for allocating a plurality of channel units to a transmission line having a plurality of timeslots including bandwidth and multiple time slot allocation. The system has a counter and a parallel to serial register for providing a channel address via an address signal corresponding to a predetermined one of the plurality of timeslots to each of the channel units. A processor is provided for assigning an assigned address to each channel unit of the plurality of channel units, such channel unit being assigned to a different selected timeslot of the plurality of timeslots. Each of the channel units has a comparator for comparing the channel address in the address signal to the assigned address, the channel unit upon having a correspondence between the channel address and the assigned address, transmitting and receiving on the transmission line. A bus connects the plurality of channel units to the means for addressing. An active channel unit can retain control of the transmission line for bandwidth and multiple time slot allocation.

15 Claims, 3 Drawing Sheets



US-PAT

DOCUM

TITLE:
transfer
disturbe
bandwid
removed

US Refe

5241632

[54] **SYSTEM FOR COMMUNICATIONS WHERE FIRST PRIORITY DATA TRANSFER IS NOT DISTURBED BY SECOND PRIORITY DATA TRANSFER AND WHERE ALLOCATED BANDWIDTH IS REMOVED WHEN PROCESS TERMINATES ABNORMALLY**

[75] Inventors: **Patrick Delaney Ross**, Sunnyvale; **Bradley David Strand**, Los Gatos; **Dave Olson**, Palo Alto, all of Calif.

[73] Assignee: **Silicon Graphics, Inc.**, Mountain View, Calif.

[21] Appl. No.: **08/805,991**

[22] Filed: **Feb. 24, 1997**

[51] **Int. Cl.**[6] **G06F 13/14**

[52] **U.S. Cl.** **395/840**; 345/841; 345/849

[58] **Field of Search** 370/232; 395/200.65, 395/232, 297, 840, 841, 849

[56] **References Cited**

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Primary Examiner—Thomas C. Lee
Assistant Examiner—Chien Yuan
Attorney, Agent, or Firm—Wagner, Murabito & Hao

[57] **ABSTRACT**

The present invention comprises a method and system for implementing prioritized communications in a computer system. The present invention is implemented on a computer system having a microprocessor and a plurality of peripheral devices coupled to the computer system. The system of the present invention determines a first priority level and determines a second priority level. The system of the present invention receives a bandwidth allocation request from a software process to transfer data at the first priority level between two or more peripheral devices. The system subsequently allocates a first priority data transfer bandwidth between the devices in response to the request and performs a first data transfer between the devices using the first priority data transfer bandwidth. In addition, the system of the present invention performs a second data transfer between other devices using a second priority data transfer bandwidth. The second data transfer occurs at a second priority level. Thus, the system of the present invention ensures the first data transfer at the first priority level is not disturbed by the second data transfer. In this manner, the system of the present invention guarantees the first priority data transfer bandwidth for the software process.

24 Claims, 15 Drawing Sheets

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